Matrox® Rapixo CXP

Installation and Hardware Reference

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Limited warranty

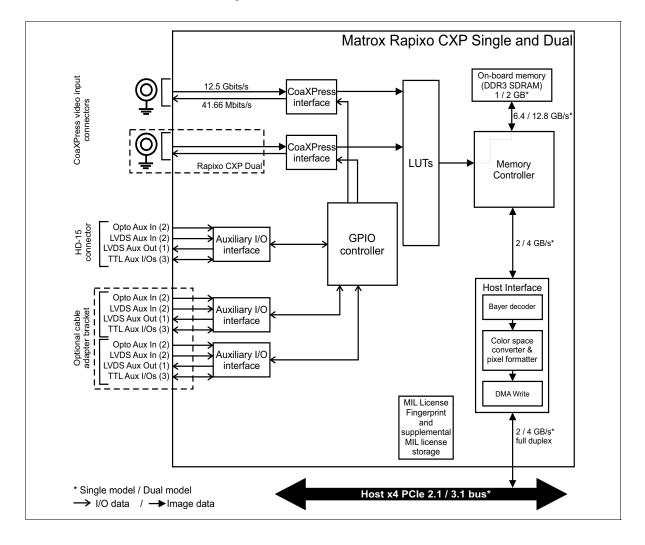
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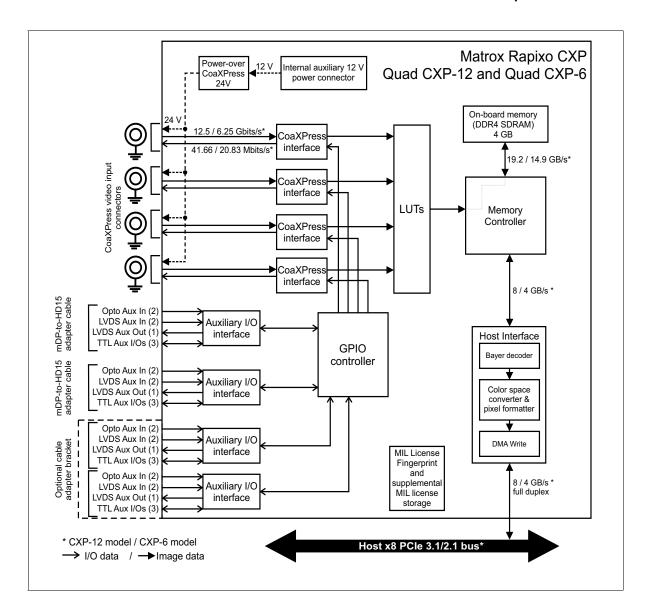
Introduction

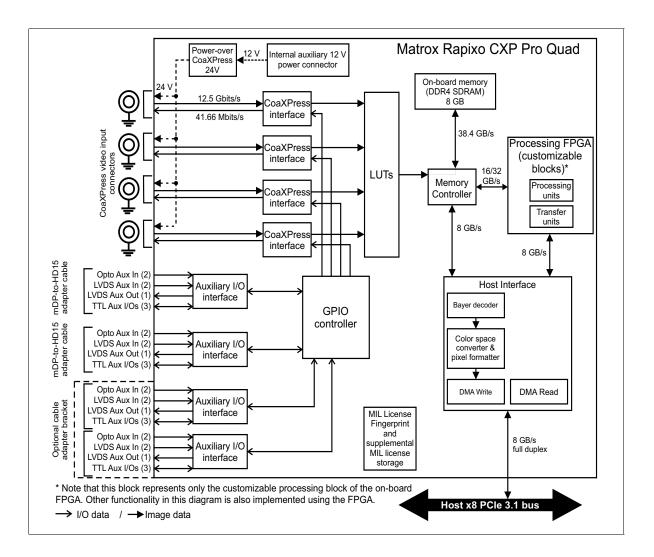
This chapter briefly describes the features of the Matrox Rapixo CXP board, as well as the software that can be used with the board.

Matrox Rapixo CXP board

Matrox Rapixo CXP is a family of high-performance PCIe frame grabbers that support image capture from high-resolution and high-speed video sources using the CoaXPress (CXP) communication standard. There are two models of the Matrox Rapixo CXP: Matrox Rapixo CXP base model and Matrox Rapixo CXP Pro. There are four versions of the base model: Single, Dual, Quad CXP-6, and Quad CXP-12. There is one version of the Pro model, the Pro Quad. The Pro model of the board also comes with FPGA-based processing-offload capabilities (a Processing FPGA).







Acquisition features with Matrox Rapixo CXP

Depending on the model, Matrox Rapixo CXP supports one, two, or four simultaneous CoaXPress links to standard CoaXPress video sources. A CoaXPress link contains all the connections and components to capture from one video source. Each connection uses one of the independent acquisition paths on Matrox Rapixo CXP. Matrox Rapixo CXP supports frame (area) and line-scan monochrome or color video sources. The color video sources can be RGB video sources or video sources with a Bayer color filter. Matrox Rapixo CXP can decode Bayer color-encoded images and perform color space conversions while transferring the image to the Host.

Matrox Rapixo CXP is available in the following CXP bit rates: 6.25 Gbits/sec (for Quad CXP-6), or 12.5 Gbits/sec (for Single, Dual, Quad CXP-12, and Pro Quad). These bit rates are the maximum per connection (depending on the cable length). Using multiple connections to implement a link (link aggregation), you can increase the bandwidth of the link to a maximum of 12.5 Gbits/sec for Single, 25 Gbits/sec for Quad CXP-6 and Dual, and 50 Gbits/sec for Quad CXP-12 and Pro Quad.

Processing capabilities

Matrox Rapixo CXP Pro features an on-board real-time processing FPGA device (Processing FPGA), which can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

Processing FPGA

The Processing FPGA on Matrox Rapixo CXP Pro is a highly customizable Xilinx Kintex UltraScale FPGA*. The operations performed on-board are controlled using the Matrox Imaging Library (MIL) application-development software. Using MIL, the processing units (PUs) of an FPGA configuration can be rearranged to perform the operations in the required sequence, without having to necessarily generate a new FPGA configuration. You would typically use standard Matrox FPGA configurations. You can also chose to implement processing on your own, using the Matrox FPGA Development Kit (FDK) and C++, or you can employ Matrox's FPGA design services to generate an application-specific FPGA configuration.

^{*.} The Processing FPGA also includes implementation for other functionality on the board, and is not used for processing only.

Before the Processing FPGA can process grabbed images, they must be stored in on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images and other data resulting from processing can be stored in on-board memory or streamed to the Host.

Additional functionality

In addition to the core video capture capabilities, Matrox Rapixo CXP incorporates a variety of features to simplify overall system integration. These features include:

- Color space converter and image formatter. This can convert data as it is being transferred to the Host. It can convert 8- or 16-bit monochrome or 24- or 48-bit packed BGR data to monochrome, packed BGR, packed BGRa, planar RGB, or YUV (YUYV) format. In addition, it can flip or subsample data sent to the Host.
- Bayer decoder. This can convert Bayer-encoded data to RGB using an average demosaicing algorithm. The following Bayer patterns are supported: GRBG, GBRG, BGGR, and RGGB.
- Auxiliary, multi-purpose signals (24 or 32 with the cable adapter bracket installed). These are non-video signals that can support one or more functionalities (for example, trigger input, rotary/linear encoder input, or timer output), depending on the auxiliary signal. With the cable adapter bracket installed, Quad CXP-6, Quad CXP-12, and Pro Quad have 32 signals available, whereas Single and Dual have 24 signals.
- **Integrated quadrature decoders.** These can decode input received from a rotary or linear encoder with quadrature output.
- Programmable lookup tables (LUTs). These allow Matrox Rapixo CXP to map data to precalculated values, before it is stored in on-board memory.
- Matrox Rapixo CXP can provide up to 13 W of power per CoaXPress connection
 to any device that supports power-over-CoaXPress (PoCXP), at a nominal voltage
 of 24 V. The internal auxiliary 12 V power connector must be connected to the
 computer's power supply cable that has a 6-pin, compatible, mating 12 V
 connector.

On-board memory

Matrox Rapixo CXP is equipped with either DDR3 or DDR4 SDRAM memory. The Single is equipped with 1 Gbyte of DDR3 SDRAM memory, and the Dual is equipped with 2 Gbytes of DDR3 SDRAM memory. Quad CXP-6 and Quad CXP-12 are equipped with 4 Gbytes of DDR4 SDRAM memory and Pro Quad is equipped with 8 Gbytes of DDR4 SDRAM memory. This memory is accessed through the memory controller, and is used to store acquired images and images for or resulting from processing. The memory controller has multiple input ports, and it has a maximum data transfer rate of 6.4 Gbytes/sec (Single), 12.8 Gbytes/sec (Dual), 14.9 Gbytes/sec (Quad CXP-6), 19.2 Gbytes/sec (Quad CXP-12), or 38.4 Gbytes/sec (Pro Quad).

Data transfer

Matrox Rapixo CXP can send data to the Host at a maximum theoretical transfer rate dependent on the model. DMA write performance is also chipset and computer dependent, and is slightly affected by the image size and alignment in Host memory (frame start address and line pitch). The theoretical transmission rates of Matrox Rapixo CXP are presented in the table below:

Matrox Rapixo CXP model	Theoretical transmission rate to Host	PCIe slot version requirement	Maximum number of lanes with a 256-payload
Single	2 Gbytes/sec	PCle 2.x	4
Dual	4 Gbytes/sec	PCle 3.x	4
Quad CXP-6	4 Gbytes/sec	PCle 2.x	8
Quad CXP-12	8 Gbytes/sec	PCle 3.x	8
Pro Quad	8 Gbytes/sec	PCle 3.x	8

To measure the effective available bandwidth of the PCIe slot in your computer with your Matrox Rapixo CXP board, Matrox provides the Matrox Rapixo CXP Bench utility. This utility is accessible using the MILConfig utility, which is shipped with software that supports Matrox Rapixo CXP (for example, MIL).

Documentation conventions

This manual refers to all Matrox Rapixo CXP boards as Matrox Rapixo CXP. When necessary, this manual distinguishes between the boards using their full names (for example, Matrox Rapixo CXP Single, Matrox Rapixo CXP Dual, Matrox Rapixo CXP Quad CXP-6, Matrox Rapixo CXP Quad CXP-12, or Matrox Rapixo CXP Pro Quad), or their abbreviated forms (Single, Dual, Quad CXP-6, Quad CXP-12, and Pro Quad). Also note that, when the term Host is used in this manual, it refers to the host computer.

Software

To operate your Matrox Rapixo CXP, you can use one or more Matrox Imaging software products that supports the board. These are the Matrox Imaging Library (MIL) and its derivatives (for example, MIL-Lite, Matrox Design Assistant, and Matrox Intellicam). All Matrox software is supported under Windows; MIL is also supported under Linux when using Matrox Rapixo CXP. Consult your software manual for supported versions of these operating systems.

MIL is a high-level programming library with an extensive set of optimized functions for image capture, processing, analysis, transfer, compression, display, and archiving. Image processing operations include point-to-point, statistical, spatial filtering, morphological, geometric transformation, and FFT operations. Analysis operations support camera calibration, are performed with sub-pixel accuracy, and include pattern recognition (normalized grayscale correlation and Geometric Model Finder), blob analysis, edge extraction and analysis, measurement, image registration, metrology, character recognition (template-based and for both normal and dot-matrix text, feature-based), code reading and verification (1D, 2D and composite code types), bead (continuous strips of material) inspection, 3D reconstruction, 3D processing, 3D analysis, classification, and color analysis.

MIL applications are easily ported to new Matrox hardware platforms and can be designed to take advantage of multi-processing and multi-threading environments.

MIL

MIL-Lite

MIL-Lite is a subset of MIL. It includes all the MIL functions for image acquisition, transfer, display control, and archiving. It also allows you to perform processing operations that are typically useful to pre-process grabbed images.

Matrox Design Assistant

The Matrox Design Assistant package is a flowchart-based, Windows program that integrates a development environment for Matrox Rapixo CXP. It allows you to create an imaging application without writing a single line of code. Application development is visually a step-by-step approach, where each step is taken from an existing toolbox and is configured through a series of dialog windows. An application developed with Matrox Design Assistant can be deployed locally (on the same computer as that used for application development) or remotely. Once the project is built and deployed, it can run without the Matrox Design Assistant interface being installed.

With Matrox Design Assistant, you can:

- Create your project as a series of steps using a flowchart.
- Test your project from your computer without any additional code editors or compilers and without deploying (copying and running) your project on the target computer.
- Design and layout a web page (operator view) to receive operator input and to display your project's output.
- Run, terminate, and re-run the project on your target computer from within Matrox Design Assistant.

Imaging projects can:

- Grab images from your camera using your Matrox Rapixo CXP.
- Analyze images using several industry-proven image analysis and measurement tools (for example, code and geometric model finder tools).
- Send and receive user-defined auxiliary I/O signals from the auxiliary I/O terminal-block connector of your Matrox Rapixo CXP.
- Send and receive information from the serial ports of your computer.

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- Send and receive information and save images across the network using the TCP/IP protocol and communicate with external devices using the Modbus or EtherNet/IP industrial protocol.
- Communicate with industrial robots to offer an integrated machine vision solution.

Matrox Intellicam

Matrox Intellicam is an interactive Windows program that allows for fast video source interfacing and provides interactive access to all the acquisition features of your Matrox boards. Matrox Intellicam also has the ability to create custom digitizer configuration format (DCF) files, which MIL and its derivatives use to interface with specific non-standard video sources. Matrox Intellicam is included with all Matrox Imaging software products.

Essentials to get started

To begin using your Matrox Rapixo CXP, you must have a computer with the following:

• An available PCIe slot with at least the following specifications if you want to operate at the maximum available bandwidth:

Model	Number of PCIe lanes required*	PCIe slot version requirement (or later)*
Single	x4	PCIe 2.x
Dual	x4	PCle 3.x
Quad CXP-6	х8	PCle 2.x
Quad CXP-12	х8	PCIe 3.x
Pro Quad	х8	PCIe 3.x

- *. Note that you can install Matrox Rapixo CXP in any mechanical PCIe slot that fits your board (for example, connecting to open-ended connectors). Be aware that if you install it in a PCIe slot that has less PCIe lanes or is of an earlier version than the capabilities of the board, then the maximum bandwidth transfer rate will be affected. For example, you can install a x8 board in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CXP and the Host is reduced by 50%.
- Processor with an Intel 64-bit architecture, or equivalent.
- MIL or one of its derivatives. This software should be installed after you install your board.

Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Consult your software package for other computer requirements (for example, operating system and memory requirements).

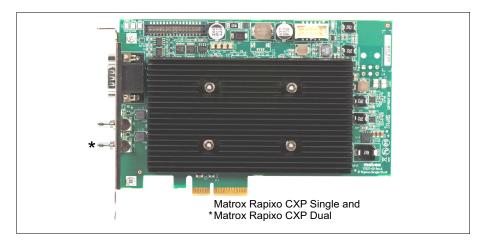
Inspecting the Matrox Rapixo CXP package

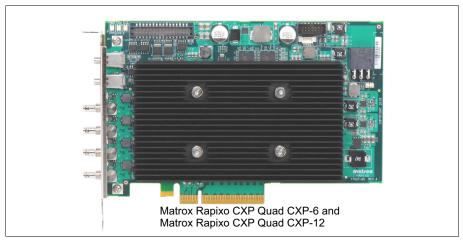
You should check the contents of your Matrox Rapixo CXP package when you first open it. If something is missing or damaged, contact your Matrox representative.

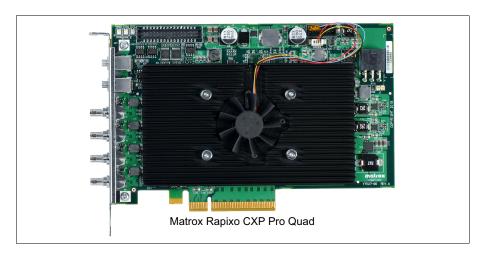
Standard items

You should receive the following items:

• The Matrox Rapixo CXP board.







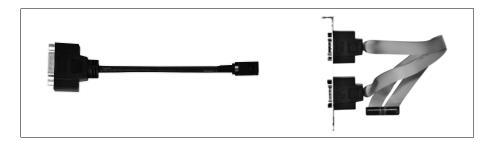
• One mDP-to-HD15 adapter cable. The cable has a mDP connector at one end, and a HD-15 connector at the other end. This cable is only available with the Quad CXP-6, Quad CXP-12, and Pro Quad.



Available separately

You might have also ordered one or more of the following:

• RAPACCKIT01. An accessory kit for the Quad CXP-6, Quad CXP-12, and Pro Quad models, which includes one mDP-to-HD15 adapter cable and one dual HD-15 I/O bracket with ribbon cable.



• RAPACCKIT02. An accessory kit for the Single and Dual models, which includes one dual HD-15 I/O bracket with ribbon cable.



- HDBNC2BNC. One 12 in (30 cm) HDBNC-male-BNC-female adapter cable.
- MIL, MIL-Lite, or Matrox Design Assistant. Matrox Intellicam is included with these software packages.
- You can purchase a 75 Ohm coaxial cables from a quality third party manufacturer, such as Belden Inc. You can also purchase a cable assembly from quality third party manufacturers such as: Hewtech, Amphenol RF, Component Express, or Oki.

Handling components

The electronic circuits in your computer and the circuits on your Matrox Rapixo CXP are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. Be sure to drain static electricity from your body by touching a metal fixture (or ground) before you touch any electronic component. In addition, do not let your clothing come in contact with the circuit boards or components.

Warning

Before you add or remove devices from your computer, always **turn off** the power to your computer and all peripherals.

Installation

The installation procedure consists of the following steps:

- 1. Complete the hardware installation procedure described in *Chapter 2: Hardware installation*.
- 2. Complete the software installation procedure described in the documentation accompanying your software package.

More information

For information on using multiple Matrox Rapixo CXP boards, refer to Chapter 3: Using multiple Matrox Rapixo CXP boards.

For in-depth hardware information, refer to *Chapter 4: Matrox Rapixo CXP hardware reference*; whereas for a summary of this information, as well as environmental and electrical specifications, and connector pinout descriptions, see *Appendix B: Technical information*.

This manual occasionally makes reference to a MIL-Lite function. However, anything that can be accomplished with MIL-Lite can also be accomplished with MIL.

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Need help?

If you experience problems during installation or while using this product, refer to the support page on the Matrox Imaging web site: www.matrox.com/imaging/support. This page provides answers to frequently asked questions, as well as offers registered customers additional ways of obtaining support.

If your question is not addressed and you are currently registered with the MIL maintenance program, you can contact technical support. To do so, you should first complete and submit the online Technical Support Request Form, accessible from the above-mentioned page. Once the information is submitted, a Matrox support agent will contact you shortly thereafter by email or phone, depending on the problem.

Chapter 2

Hardware installation

This chapter explains how to install your Matrox Rapixo CXP board in your computer.

Installing your Matrox Rapixo CXP board

Before you install your Matrox Rapixo CXP board, some precautionary measures must be taken. Turn off the power to your computer and its peripherals, and drain static electricity from your body (by touching a metal part of the computer chassis).

Important

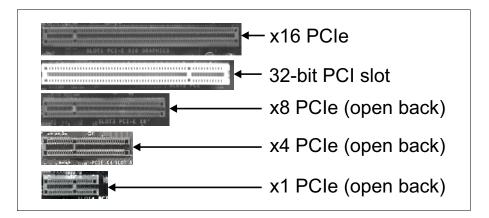
❖ Note that your board should be installed before you install your software.

Proceed with the following steps to install your board:

- 1. Remove the cover from your computer; refer to your computer's documentation for instructions.
- 2. Check that you have an empty PCIe slot in which to install your board. For maximum available bandwidth:

Model	Number of PCle lanes required*	PCIe slot version requirement (or later)*
Single	x4	PCIe 2.x
Dual	x4	PCle 3.x
Quad CXP-6	х8	PCle 2.x
Quad CXP-12	х8	PCle 3.x
Pro Quad	х8	PCIe 3.x

*. Note that you can install Matrox Rapixo CXP in any mechanical PCIe slot that fits your board (for example, connecting to open-ended connectors). Be aware that if you install it in a PCIe slot that has less PCIe lanes or is of an earlier version than the capabilities of the board, then the maximum bandwidth transfer rate will be affected. For example, you can install a x8 board in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CXP and the Host is reduced by 50%.

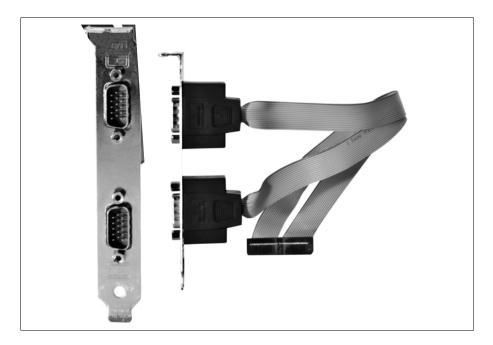


Matrox Rapixo CXP might drop frames if the PCIe slot has less active lanes than the capabilities of the board (for example, if a Quad CXP-12 is connected to a x8 PCIe slot that has only four active lanes*). Verify with your motherboard manufacturer to find out whether your motherboard works efficiently with a x4 or x8 PCIe board, such as Matrox Rapixo CXP (for example, whether the PCIe slots are wired for x4 or x8 boards).

If you need to install the HD-15 cable adapter bracket, you will need an additional slot. This slot does not need to be adjacent to the Matrox Rapixo CXP board. In addition, the cable adapter bracket does not plug into a slot's connector; it attaches only to the back of the computer's chassis.

^{*.} After installing the board, you can verify in software the number of PCIe lanes that are currently active, using the MIL-Lite function MsysInquire() with M_PCIE_NUMER_OF_LANES. You can also verify this through the MILConfig, utility on the **Boards** page.

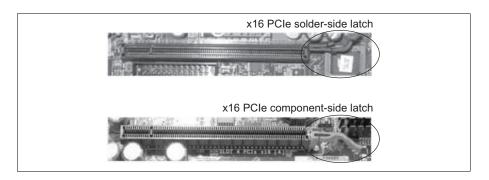
❖ Note that the external auxiliary I/O connectors on the cable adapter bracket are panel mount connectors. If you don't want to occupy an entire slot for the bracket, you can punch out two holes in the computer chassis, and then screw the connectors in the holes.



- 3. If there is a metal plate at the back of the selected slots, remove it. Keep the screw from the top of the plate to anchor your board and cable adapter bracket once they are installed.
- 4. Position your Matrox Rapixo CXP board in the selected PCIe slot. Align the connectors of your board with the opening at the back of the slot, and move the board until the connectors pass through the opening.

Important

When installing your Matrox Rapixo CXP board in a x16 PCIe slot, special care must be taken to avoid damaging the board. Some x16 PCIe slots have a connector with a retainer. You should avoid touching the latch of this retainer with the board. Alternatively, you can remove the latch from the retainer.



- 5. Once the input connectors are in the opening of the chassis, press the board firmly but carefully straight down into the connector of the slot.
- 6. Anchor the board using the screw that you removed in step 3.
- 7. Optionally, for Quad CXP-6, Quad CXP-12, and Pro Quad, connect your computer's power supply cable that has a 6-pin, compatible, mating 12 V connector, to the internal auxiliary 12 V power connector.
 - * You only need to connect the auxiliary power if you are using PoCXP-compliant video sources with Matrox Rapixo CXP.
- 8. If required, install the cable adapter bracket, as described in the section *Installing the cable adapter bracket*, later in this chapter.
- 9. Attach your video sources.
- 10. Turn on your computer.
 - When you boot your computer under Windows, Windows' Plug-and-Play system will detect a new Multimedia Video Device and you will be asked to assign it a driver. At this point, you should click on Cancel.

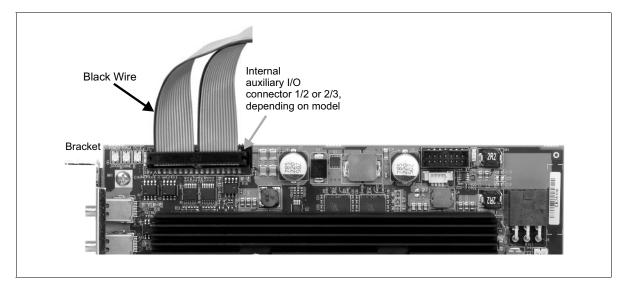
Under Windows and Linux, the driver will be installed during the installation of Matrox Rapixo CXP software.

- 11. Disable active state power management (ASPM) for PCIe devices, to maximize the performance of Matrox Rapixo CXP. In the BIOS, disable all ASPM (or equivalent) settings (typically accessible from the **Power management** sub-menu of the Advanced Configurations menu). In addition, if the operating system has an ASPM for PCIe devices option, disable this option as well. For example, under Microsoft Windows 10, open the **Power Options** dialog box from the Windows Control Panel. For the currently selected power plan, click on Change Plan Settings and then click on Change Advanced Power Settings. In the presented dialog, expand PCI Express, and then expand Link State Power Management and set it to Off.
- 12. Under Microsoft Windows, set the power plan option to high performance to maximize the performance of Matrox Rapixo CXP and minimize the possibility of dropped frames. For example, under Microsoft Windows 10, open the **Power** Options dialog box from the Windows Control Panel and set the power plan option to High Performance.

Installing the cable adapter bracket

To install the cable adapter bracket, proceed with the following steps:

- 1. Make sure that your Matrox Rapixo CXP board is fastened to the computer chassis.
- 2. Attach the cable adapter bracket to internal auxiliary I/O connector 1/2 or 2/3 on the Matrox Rapixo CXP board. When attaching the flat ribbon cables of the adapter bracket, position the cable so that the black wire is on the same side as the bracket of the Matrox Rapixo CXP board.



- 3. Slide the bracket of the cable adapter bracket into the opening at the back of the selected slot.
- 4. Anchor the bracket to the chassis using the screw that you removed in the previous section.

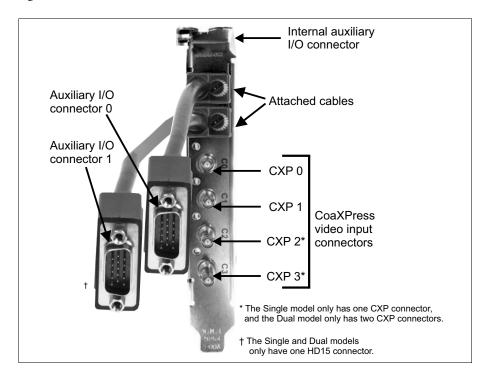
Note that the external auxiliary I/O connectors on the cable adapter bracket are panel mount connectors. If you don't want to occupy an entire slot for the additional bracket, you can punch out two holes in the computer chassis, and then screw the connectors in the holes.

^{*.} This wire could be black or any other color.

Connecting video sources to Matrox Rapixo CXP

The Matrox Rapixo CXP board has the following connectors on its bracket:

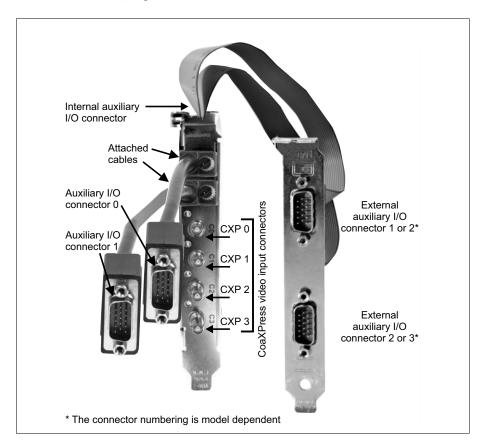
- CoaXPress video input connector(s). Used to receive video streams from the CoaXPress video sources. These connectors are also used to transmit CoaXPress trigger signals, as well as transmit and receive control and acknowledgment messages.
- mDP connector(s). These connectors are found on the Quad CXP-6, Quad CXP-12, and Pro Quad models and are used to connect the mDP-to-HD15 adapter cable. The HD-15 connector on the adapter cable is called an external auxiliary I/O connector. This connector is used to transmit and receive auxiliary signals.



• HD15 connector. This connector is found on the Single and Dual models and is used to transmit and receive auxiliary signals.

To access the signals of internal auxiliary I/O connector 2/3, you can install the cable adapter bracket.

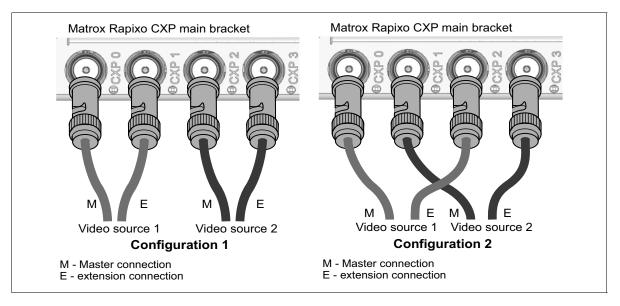
• External auxiliary I/O connectors (panel mount HD-15). Each used to transmit and receive auxiliary signals.



Connecting to the CoaXPress video input connectors

When attaching video sources to your Matrox Rapixo CXP, you must use 75 Ohm, coaxial cables with a 12G rated HD-BNC male connector (plug). For the best performance, it is recommended that you use high-quality cables, such as Belden 1694A cables (which are good for typical cable lengths), or Belden 4794R cables (which maintain signal quality at greater lengths).

Note that a video source with multiple cables will have one master connection (typically attached to connector 1 on the camera) and the others as extension connections. Keep track of the video input connector to which you attach the master connection because you will need this information when using MIL-Lite (MdigAlloc() with M_DEVn) to identify the video source.



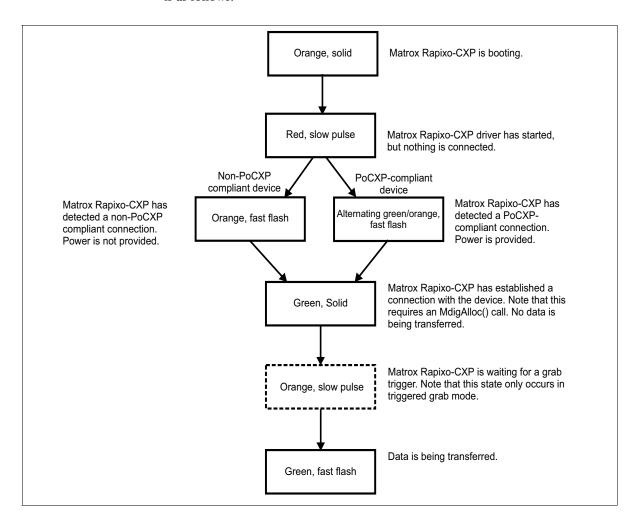
Matrox Rapixo CXP communicates with the video sources to identify which video source is connected to which input connectors.

Note that if you are using more than one coaxial cable to connect to the same video source, the cables you choose must be of the same type and length.

The length of cable that you choose will affect the maximum data transmission rate. In general, for lengths greater than 40 m, the longer your cables, the lower the maximum possible bit rate. For example, when using high-quality, 100 m cables, the maximum possible bit rate is 3.125 Gbits/sec. Another factor that affects the bit rate is the quality of the cables that you choose.

CoaXPress LEDs

The four CoaXPress LEDs on the main bracket identify the state and activity of connected devices. The LEDs respect the JIIA CoaXPress Standard version 2.0 specification for connector indicator lamps. The typical sequence of LED states is as follows:



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This is a typical sequence for the LED states on your Matrox Rapixo CXP. Refer to the *CoaXPress LEDs* section in *Appendix B: Technical information* for the complete list of possible LED states.

The following identifies the different timing used to define the LED flash or pulse states that can occur:

LED indication	Hz	Timing (+/- 20%)
Fast flash	12.5	20 msecs on, 60 msecs off
Slow flash	0.5	1 sec on, 1 sec off
Slow pulse	1	200 msecs on, 800 msecs off

Chapter 8

Using multiple Matrox Rapixo CXP boards

This chapter explains how to use multiple Matrox Rapixo CXP boards.

Installation of multiple boards

You can install and use multiple Matrox Rapixo CXP boards in one computer.

Install each additional Matrox Rapixo CXP board the same way you installed the first board (refer to Chapter 2: Hardware installation). The number of Matrox Rapixo CXP boards that you can install is primarily dependent on the number of physical slots in your computer, and your BIOS; your BIOS establishes how many PCIe devices can be mapped to the PCIe memory space of your computer.

Using MIL-Lite, you have to allocate a MIL system for each board and allocate the resources of each MIL system. For more information, see MsysAlloc() with M_SYSTEM_RAPIXOCXP in the MIL Reference.

Simultaneous image capture from different boards

In addition to capturing images from multiple video sources with a single Matrox Rapixo CXP board, you can also simultaneously capture images from video sources attached to multiple Matrox Rapixo CXP boards. Note that the number of video sources from which you can simultaneously capture images is limited by the PCIe chipset on your computer.

Depending on the model of Matrox Rapixo CXP, a high performance PCIe chipset might be necessary to sustain PCIe transfers to Host memory. Ideally, the Single and Quad CXP-6 models should use at least a PCIe 2.x chipset and the Dual, Quad CXP-12, and Pro Quad models should use at least a PCIe 3.x chipset. Using the correct PCIe chipset will optimize the speed of data transmission and will minimize data loss. The list of platforms that are known to be compatible with Matrox Rapixo CXP is available on the Matrox web site, under the board's compatibility list.

To measure the effective available bandwidth of the PCIe slot in your computer with the Matrox Rapixo CXP board, you can use the Matrox Rapixo CXP Bench tool, accessible using the MILConfig utility. As a reference point, capturing from a 2K x 2K, 8-bit, 60 frames/sec video source will require a minimum bandwidth of 240 Mbytes/sec, plus an additional bandwidth margin of approximately 20%, for a bandwidth of 288 Mbytes/sec.

Chapter

4

Matrox Rapixo CXPhardware reference

This chapter explains the architecture, features, and modes of the Matrox Rapixo CXP hardware.

Matrox Rapixo CXP hardware reference

This chapter provides information on the Matrox Rapixo CXP hardware. It covers the architecture, features, and modes of the board's acquisition section. In addition, the chapter covers the Matrox Rapixo CXP hardware related to the formatting and transfer of data. A summary of the features of Matrox Rapixo CXP, as well as pin assignments for the various connectors, can be found in *Appendix B: Technical information*.

Acquisition path

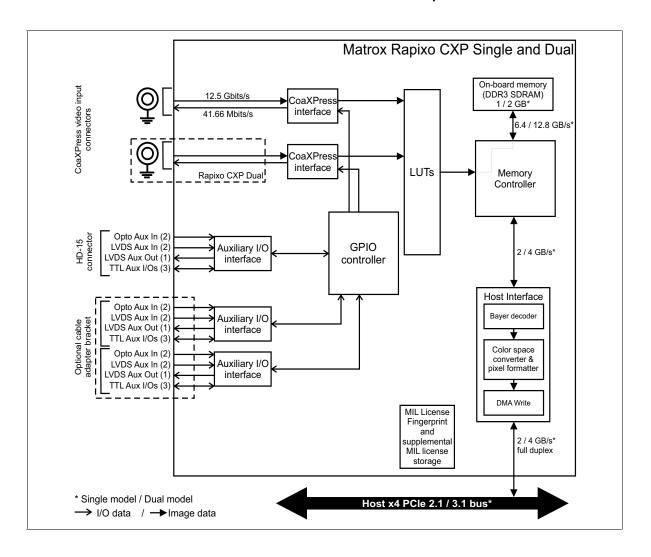
This manual uses the term acquisition path to refer to a path that has the capability to, for example, capture a component or stream of the video input signal. The term *independent acquisition path* is used to refer to an acquisition path that can, if required, acquire data from a video source independently from another such path on the same frame grabber. On Matrox Rapixo CXP, each CoaXPress connection in a CoaXPress link uses a different acquisition path.

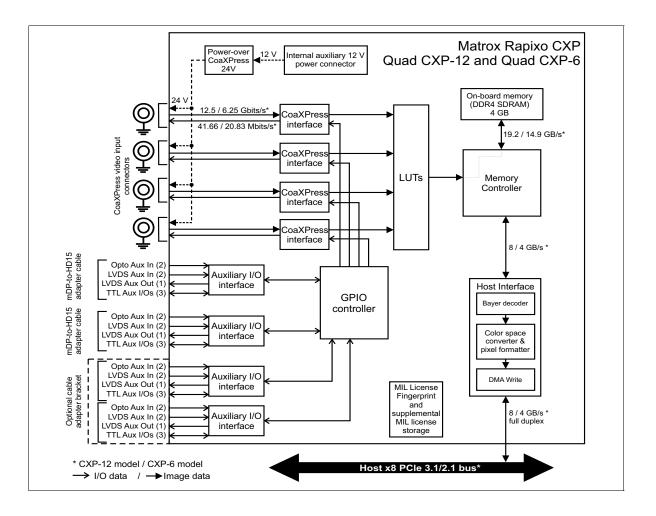
Digitizer

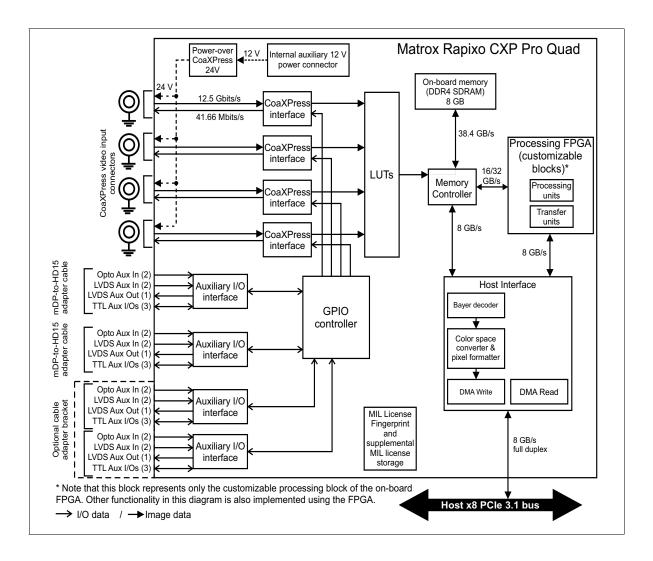
MIL-Lite uses the concept of a MIL digitizer to represent the acquisition path(s) with which to grab from one input source (one CoaXPress link on Matrox Rapixo CXP) of the specified type. When several MIL digitizers are allocated, their device number along with their DCF identify if they represent the same path(s) (but perhaps for a different input format) or independent path(s) for simultaneous acquisition.

Digitizer configuration format

To program the acquisition section, allocate a MIL digitizer using MdigAlloc() with an appropriate DCF (supplied or created) and digitizer device number. If you find a DCF file that is suitable for your video source, but you need to adjust some of the more common settings, you can do so directly, without adjusting the file, using the appropriate MIL-Lite function. For more specialized adjustments, use the Matrox Intellicam program to adjust the DCF file.







Matrox Rapixo CXP acquisition

Matrox Rapixo CXP can capture video from digital video sources compliant with the CoaXPress standard 2.0 specification (as well as 1.1 and 1.1.1). Depending on the model, Matrox Rapixo CXP has one, two, or four independent acquisition paths (CoaXPress connections). When a video source is connected to Matrox Rapixo CXP, the board communicates with the video source to determine the rate at which data will be transferred. Matrox Rapixo CXP can provide power-over-CoaXPress to attached video sources.

For each video source connected to the board, Matrox Rapixo CXP supports a CoaXPress trigger output signal, which is used to communicate exclusively with the video source. To communicate with other third-party devices, Matrox Rapixo CXP provides 24 or 32 auxiliary signals (depending on the model). Auxiliary input signals can be rerouted to the CoaXPress trigger output signal and the CoaXPress trigger input signal can be rerouted to auxiliary output signals.

Matrox Rapixo CXP supports monochrome, RGB color, and Bayer color-encoded acquisition. The board can perform color-conversion, flipping, and image subsampling.

Performance

The maximum data transmission rate that you can achieve depends on the length of your coaxial cable, the quality of the cable, your video source, as well as the type of PCIe slot in which you install your Matrox Rapixo CXP.

	Quad CXP-6 maximum	Single, Dual, Quad CXP-12 and Pro Quad maximum
Number of pixels/line	64K	64K
Number of lines/frame	64K	64K
Data transfer bit rate from camera (per connection)	Up to 6.25 Gbits/sec	Up to 12.5 Gbits/sec
Data transfer bit rate to camera (per connection)	Up to 20.83 Mb/sec	Up to 41.66 Mb/sec

Effect of cable length

For lengths greater than 40 m, the longer the cables, the lower the maximum possible bit rate. High-quality cables, such as Belden 1694A cables or Belden 4794R cables, will allow for the highest possible bit rates. The table below outlines the bit rates that you can expect to achieve at certain lengths, using Belden 1694A cables, as well as the bit rates possible when connecting to a single video source using link aggregation (2, 3, and 4 cables).

Length	Number of connections to video source	Maximum bit rate
130 m	1	1.25 Gbits/sec
100 m	1	3.125 Gbits/sec
60 m	1	6.25 Gbits/sec
40 m	1	12.5 Gbits/sec
40 m	2	25.0 Gbits/sec
40 m	4	50.0 Gbits/sec

Effect of the type of PCIe slot

Both the version and number of active lanes of your PCIe slot are important to consider. A PCIe 3.x slot supports a higher data transmission rate than a 2.x slot; furthermore, a x8 PCIe slot will double the data rate, when compared to a x4 PCIe slot of the same base specification (3.x or 2.x). The Dual, Quad CXP-12, and Pro Quad models require a 3.x slot to operate at the maximum available bandwidth. While transferring data to the Host, these factors will reduce the maximum transmission rate as follows.

PCIe slot	Theoretical	Estimated maximum practical transmission rate							
base specifications	transmission rate per lane	х4	х8						
PCIe 2.x	500 Mbytes/sec	1.75 Gbytes/sec	3.5 Gbytes/sec						
PCIe 3.x	1 Gbytes/sec	3.5 Gbytes/sec	7 Gbytes/sec						

Power-over-CoaXPress

Matrox Rapixo CXP supports power-over-CoaXPress (PoCXP) compliant video sources, and non-PoCXP compliant video sources. Matrox Rapixo CXP can provide up to 13 W per connection, at a nominal voltage of 24 V, to the devices connected to the CoaXPress input connectors. The Quad CXP-6, Quad CXP-12, and Pro Quad models require connection to the computer's power supply cable with a 6-pin, compatible, mating 12 V connector to provide power-over-CoaXPress (PoCXP). The Single and Dual models use power from the PCIe slot provide power-over-CoaXPress (PoCXP) and do not need to be connected to an external power supply.

Matrox Rapixo CXP detects whether the video source is PoCXP-compliant. When connecting to non-PoCXP compliant video sources, Matrox Rapixo CXP has appropriate circuitry to ensure that no power is transmitted. To manually disable the PoCXP circuitry and ensure that no power is sent to the device, you can use the MIL-Lite function MdigControl() with M_POWER_OVER_CABLE.

Matrox Rapixo CXP is also equipped with an overcurrent protection mechanism; if this fails, there is also a resettable fuse that can sustain a current of 1 A.

Acquisition

Matrox Rapixo CXP accepts 8-, 10-, 12-, and 16-bit video data. All data is transmitted in packets over a CoaXPress link.

The Matrox Rapixo CXP CoaXPress interface is responsible for decoding packets from the video sources, as well as buffering incoming data before it is written to memory. Video sources can be frame or line-scan video sources.

CoaXPress trigger signals and control messages

To communicate exclusively with the video source(s), Matrox Rapixo CXP supports CoaXPress trigger signals going to the camera and control messages. Trigger packets, which are sent to the camera, are virtually represented as trigger signals. Control messages constitute the basic communication mechanism between the video source(s) and the board.

For each video source connected to the board, Matrox Rapixo CXP supports a CoaXPress trigger output signal. A CoaXPress trigger output signal can be sent from the board to a video source to initiate image acquisition or to optionally control the exposure time.

For data coming from the camera (downlink) at speeds of up to 6.25 Gbits/sec (Quad CXP-6), the maximum trigger rate is approximately 150 KHz; for data coming from the camera at speeds of 12.5 Gbits/sec (Single, Dual, Quad CXP-12, and Pro Quad), the maximum trigger rate is approximately 300 KHz. Depending on your camera, you might have the ability to double the trigger rate. See your camera's documentation for more details.

To send a trigger output signal to the camera, you use the MIL-Lite function MdigControl() with M_IO_SOURCE + M_TL_....For more information on how to use the auxiliary input and output signals, refer to the *Auxiliary signals* section, later in this chapter.

Auxiliary signals

This section describes the auxiliary signals available on Matrox Rapixo CXP.

Auxiliary signals available on Matrox Rapixo CXP

The auxiliary signals of Matrox Rapixo CXP are acquisition path independent and can be used to initiate on-board events (inputs) or can be transmitted to third-party devices (outputs). You can also reroute an auxiliary input signal to a video source via the CoaXPress trigger output signal.

The following table summarizes the auxiliary functionality that Matrox Rapixo CXP supports using its auxiliary I/O signals. The table also documents the MIL constants to use.

		TTL Aux I/O					OPTO Aux In					LVDS Aux In						LVDS Aux Out														
				ı	Aux I	/0 (onn	ecto	r				Aux I/O Connector				Aux I/O Connector					Aux I/O Connector			r							
		0			1			2			3*		(0		1	:	2	3	*	-)		1	:	2	3	*	0	1	2	3*
M_AUX_IOn [†]	4	5	6	12	13	14	20	21	22	28	29	30	0	1	8	9	16	17	24	25	2	3	10	11	18	19	26	27	7	15	23	31
Functionality that can be routed or received	AUX(TRIG)_TTL_I0_4	AUX(TRIG)_TTL_I0_5	AUX(TRIG)_TTL_I0_6		ог ⁻ тт-	AUX(TRIG)_TTL_I0_14	o'_ □_ □_	AUX(TRIG)_TTL_10_21	AUX(TRIG)_TTL_I0_22	_TTL_10_	AUX(TRIG)_TTL_10_29	AUX(TRIG)_TTL_I0_30	AUX(TRIG)_OPTO_IN0	AUX(TRIG)_0PT0_IN1	AUX(TRIG)_0PT0_IN8	AUX(TRIG)_OPTO_IN9	AUX(TRIG)_0PT0_IN16	AUX(TRIG)_0PT0_IN17	AUX(TRIG)_0PT0_IN24	AUX(TRIG)_0PT0_IN25	AUX(TRIG)_LVDS_IN2	AUX(TRIG)_LVDS_IN3	AUX(TRIG)_LVDS_IN10	AUX(TRIG)_LVDS_IN11	AUX(TRIG)_LVDS_IN18	AUX(TRIG)_LVDS_IN19	AUX(TRIG)_LVDS_IN26	AUX(TRIG)_LVDS_IN27	AUX(EXP)_LVDS_0UT7	AUX(EXP)_LVDS_0UT15	AUX(EXP)_LVDS_0UT23	AUX(EXP)_LVDS_0UT31
Timer (M_TIMERn [†])	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4																	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4	1/2/ 3/4
Trigger controller affected by input signal	‡	†	†	t	t	t	t	t	†	†	t	†	†	t	t	†	t	t	t	†	†	†	t	t	t	†	t	†				
Bit of rotary0																					0	1										
input§ 1 2																							0	1	•							
2 3																									0	1	0	1				
User output (bit of static-user-output register M_USER_BITn [†])	4	5	6	12	13	14	20	21	22	28	29	30															J	,	7	15	23	31

- *. These signals are not available on the Single and Dual models.
- †. MIL constant, where *n* corresponds to the number in the row.
- ‡. There is no limit to the number of events that can be triggered simultaneously using the auxiliary input signals, nor is there a restriction on which auxiliary signal can be used to trigger an event.
- §. A rotary encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

Specifications of the auxiliary signals

Matrox Rapixo CXP has auxiliary signals in the following formats:

	Total # of signals						
Signal Format	From each mDP or DB15 connector	From cable brackets					
TTL auxiliary input or output signals	3	6					
Opto-isolated auxiliary input signals	2	4					
LVDS auxiliary input signals	2	4					
LVDS auxiliary output signals	1	2					
Total number of auxiliary signals	8	16					

When you route an external signal to an auxiliary signal or vice versa, verify that the external signal meets the electrical specifications of the auxiliary signal.

When an auxiliary input signal is received in TTL format directly, it will be clamped at a maximum of 5.7 V and at a minimum of -0.7 V to protect the input buffer. Typically, the signal should have a maximum of 5 V and a minimum of 0 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low.

The opto-isolated auxiliary input signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and allows the frame grabber to be totally isolated. The voltage difference across the positive and negative components of the signal must be between 4.71 V and 9.165 V for logic high, and between 0 V (recommended) and 0.8 V for logic low.

You can set the direction of an auxiliary I/O signal using the MIL-Lite function MdigControl() with M_AUX_SIGNAL_MODE.

You can set up the auxiliary signals in the DCF. Alternatively, for most commonly used functionalities, you can configure the auxiliary signals using the MIL-Lite function MdigControl() (for example, with M_IO..., M_GRAB_TRIGGER..., M_TIMER..., or M_ROTARY_ENCODER...).

Timers

Matrox Rapixo CXP has 4 16-bit timers, which operate based on a specified clock source. Timer output signals allow you to control the exposure time and other external events related to the video source (such as a strobe). A timer output signal can be output on any of the auxiliary output signals or auxiliary I/O signals in output mode. A timer output can also be sent to a video source via the CoaXPress trigger output signal.

The timers can use one of the following as a clock source:

- A 125MHz internal clock source.
- A clock based on the output of another timer set in continuous mode.
- A clock based on the HSYNC or VSYNC signal of your camera.
- A clock based on the pixel clock signal of your camera.

To route a timer output on an auxiliary signal, use the MIL-Lite function MdigControl() with M_IO_SOURCE + M_AUX_IOn set to M_TIMERn. To set up a timer, use MdigControl() with M_TIMER_....

Trigger

You can use as a trigger any of the auxiliary input signals (or auxiliary I/O signals in input mode), or the CoaXPress trigger input signal. A trigger signal can be used to initiate image acquisition or prompt an on-board event.

To enable grabbing upon a trigger, use the MIL-Lite function MdigControl() with M_GRAB_TRIGGER_STATE. To set the signal used to trigger the grab, use MdigControl() with M_GRAB_TRIGGER_SOURCE. To start a timer upon a trigger, use MdigControl() with M_TIMER_TRIGGER_SOURCE.

Quadrature decoder

Matrox Rapixo CXP features 4 quadrature decoders. They are used to decode quadrature input received from linear or rotary encoders with a quadrature output. A rotary encoder is a device that provides information about the position and direction of a rotating shaft (for example, that of a conveyor belt); a linear encoder is a device that provides information about the position and direction of a moving sensor along a scale. Encoders with quadrature output transmit a two-bit code (also known as Gray code) on two pairs of LVDS wires for each change in position

of the rotating shaft, or of the sensor along the scale. For a given direction, the encoder outputs the code in a precise sequence (either 00 - 01 - 11 - 10 or 00 - 10 - 11 - 01, depending on how the encoder is attached. If the rotating shaft, or sensor moving along the scale, changes direction, the encoder transmits the Gray code in the reverse sequence (00 - 10 - 11 - 01 or 00 - 01 - 11 - 10, respectively).

Upon decoding a Gray code, the rotary decoder increments or decrements its 32-bit internal counter, depending on the direction of movement. You can configure which Gray code sequence represents forward movement and increments the counter; the reverse Gray code sequence will then represent the backward direction and decrement the counter. You can specify the direction of movement occurring when the Gray code sequence is 00 - 01 - 11 - 10, using MdigControl() with M_ROTARY_ENCODER_DIRECTION.

The rotary decoder supports encoder frequencies of up to 50 MHz. The encoders can only be connected to our LVDS auxiliary input signals. The LVDS receivers on Matrox Rapixo CXP can support, under most circumstances, RS-422 signaling; refer to the electrical specification of the LVDS auxiliary input signals in *Appendix B: Technical information* for requirements.

❖ Note that an external source must be used to power the rotary or linear encoder.

You can configure the rotary decoder's settings, using the MIL-Lite function MdigControl() with M_ROTARY_ENCODER..., or by modifying the DCF file with Matrox Intellicam.

User signals

Auxiliary signals can also be used to transmit or receive application-specific user output and/or input.

If you want to start or stop an external event based on some calculation or analysis, you can manually set the state of any auxiliary output signal (or I/O signal set to output) to high or low. To do so, you set the state (on/off) of a bit in a user settable register (static-user-output register). When the bit is on, its associated auxiliary output signal will be high; when it is off, the auxiliary output signal will be low. This bit is referred to as a user-bit. To route the state of a user-bit to an auxiliary output signal, use MdigControl() with M_IO_SOURCE and M_USER_BITn; to set the state of a user-bit, use MdigControl() with M_USER_BIT_STATE.

Your application can also act upon and interpret the state of an auxiliary input signal (or I/O signal set to input). The state of an auxiliary input signal is not associated with a user-bit; you poll the state of the signal directly. To poll the state of an auxiliary input signal, use MdigInquire() with M_IO_STATUS. The state of an auxiliary input signal can also generate an interrupt; to do so, use MdigControl() with M_IO_INTERRUPT_STATE and then use MdigHookFunction() with M_IO_CHANGE to hook a function to this event (that is, to set up an event handler).

On-board memory

Matrox Rapixo CXP is equipped with on-board memory that is model dependent. This memory is accessed through the memory controller, and is used to store acquired images and images for or resulting from processing (Pro Quad). The table below describes the memory and transfer rates available on different Matrox Rapixo CXP models.

Matrox Rapixo CXP model	On-board memory	Maximum theoretical transfer rate				
Single	1 Gbyte DDR3	6.4 Gbytes/sec				
Dual	2 Gbytes DDR3	12.8 Gbytes/sec				
Quad CXP-6	4 Gbytes DDR4	14.9 Gbytes/sec				
Quad CXP-12	4 Gbytes DDR4	19.2 Gbytes/sec				
Pro Quad	8 Gbytes DDR4	38.4 Gbytes/sec				

Matrox Rapixo CXP has a default of 128 Mbytes of on-board memory mapped onto the PCIe bus. You can use a Host pointer to access this memory, or you can access it directly from another PCIe bus master; this memory is referred to as shared memory. To allocate a buffer in shared memory, use the MIL-Lite function MbufAlloc...() with M_ON_BOARD + M_SHARED.

Note that, the shared memory size can be modified for the Quad CXP-6, Quad CXP-12, and Pro Quad models. For the Single and Dual models, the memory size is fixed and cannot be modified.

Data conversion

Data can be modified both before it is saved to on-board memory and as it is being transferred to the Host. For the Pro Quad model, if you need to modify the data after it has been saved to on-board memory and before it is transferred to the Host, you will need to include appropriate processing units (PU) in your FPGA configuration.

Lookup tables

Matrox Rapixo CXP has on-board lookup tables (LUTs) that can precondition input data at acquisition time, before it is stored in on-board memory.

The on-board programmable lookup tables (LUTs) can map 8-bit, 10-bit, and 12-bit data (monochrome or color). When a link is receiving color data, all bands of the data use the same specified LUT mapping. As soon as one link is receiving 12-bit data, all links (CoaXPress connections) share the same specified LUT mapping. Data of other depths are mapped through transparent LUTs. The LUTs are programmed using the MIL-Lite function MdigControl() with M_LUT_ID.

Bayer color decoder

As data from on-board memory is transmitted to the Host, it can pass through the Bayer color decoder. The Bayer color decoder converts Bayer color encoded images (GB, BG, GR, and RG pattern support) to multi-band RGB images using a 2x2 average demosaicing algorithm.

Color space converter and image formatter

As data from on-board memory, processing, or the Bayer color decoder is transmitted to the Host, it passes through the color space converter and image formatter. The color space converter and image formatter can convert data in the following ways:

• Subsampling. Image data can be subsampled.

The color space converter and image formatter can subsample in the horizontal and vertical directions by integer factors of 1 to 16. The color space converter and image formatter uses nearest-neighbor interpolation.

You can use any of the following MIL-Lite functions to subsample image data:

- MdigControl() with M_GRAB_SCALE_X/Y and the subsampling factor.

- MimResize() with ScaleFactorX and ScaleFactorY and the subsampling factor.
- **MbufTransfer**() with **M_COPY** + **M_SCALE** and setting the destination buffer size smaller than the original image.

Note that Matrox Rapixo CXP does not support cropping in hardware. However, you can have image data cropped during transfer to Host using MdigControl() with M_SOURCE_SIZE_X/Y and M_SOURCE_OFFSET_X/Y.

- Flipping. Images can be flipped horizontally or vertically, using the MIL-Lite function MdigControl() with M_GRAB_DIRECTION_X/Y or when calling MimFlip() from on-board buffer to Host.
- Color space conversion. The color space converter and image formatter formats an image based on its type and the bit-depth and color format of the destination buffer. You can set the bit depth and color format of the destination buffer when you allocate it using the MIL-Lite function MbufAlloc...(). The format of the source image is established in the DCF.

Image data can be converted as follows:

Input format		Output format							
	8-bit monochrome	16-bit monochrome	24-bit packed BGR	32-bit packed BGRa	48-bit packed BGR	16-bit YUV (YUYV)	24-bit RGB planar	48-bit RGB planar	
8-bit monochrome	yes		yes	yes		yes	yes		
16-bit monochrome	yes	yes	yes	yes	yes	yes	yes	yes	
24-bit packed BGR	yes		yes	yes		yes	yes		
48-bit packed BGR	yes	yes	yes	yes	yes	yes	yes	yes	

The equations for the YUV16 conversion are described in the following table. The value of *depth* is either 8 or 16 when converting BGR24 or BGR48 data, respectively. Note that while performing BGR48-to-YUV color space conversion, the operations are carried out on 16-bit data; then, each resulting YUV component is bit-shifted right by 8 bits (>> (*depth* - 8) where the value of *depth* is 16).

Color space conversion	Equations
BGR-to-YUV	• Y = (0.114B + 0.587G +0.299R) >> (depth - 8)
	• U = $(0.500B - 0.331G - 0.169R + 2^{(depth-1)}) >> (depth - 8)$
	• $V = (-0.081B - 0.419G + 0.500R + 2^{(depth-1)}) >> (depth - 8)$

Processing FPGA

To reduce the number of image processing tasks that the Host CPU must perform, the Pro Quad model has a Processing FPGA. The Processing FPGA on the Pro Quad model is a highly customizable Xilinx Kintex UltraScale* (KU035 or KU060). The Processing FPGA can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

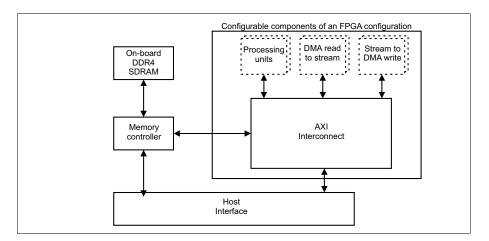
Before the Processing FPGA can process grabbed images, they must be stored in on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images and other data resulting from processing can be stored in on-board memory or streamed to the Host.

The maximum peak bandwidth for images streamed directly to/from Host memory is 8 Gbyte/sec, as well as for images streamed to/from on-board memory.

^{*.} Other functionality is also implemented through the FPGA, besides customizable processing, such as the timers and quadrature decoders.

Possible processing operations

To use the Processing FPGA, you must configure it with an FPGA configuration that defines the appropriate functionality. An FPGA configuration is a code segment that is used to program an FPGA. The following diagram shows the configurable FPGA components in an FPGA configuration.



You would typically use standard Matrox FPGA configurations. You can also chose to implement processing on your own, using the Matrox FPGA Developers Toolkit (FDK) and C++. If required, Matrox's FPGA design services can be employed to develop an application-specific FPGA configuration.

Once the Processing FPGA is programmed, you can then make use of its functionality using MIL. Refer to *Using MIL with a Processing FPGA* chapter in the *MIL User Guide* for more information.

Host interface

The Matrox Rapixo CXP PCIe Host interface is capable of high-speed DMA transfers to Host memory, or other memory mapped onto the PCIe bus. The DMA write engine of the Host interface is capable of performing the transfers without the help of the Host CPU. The PCIe slot version and maximum number of PCIe lanes of Matrox Rapixo CXP are presented in the table below:

Matrox Rapixo CXP model	Theoretical transmission rate to Host	PCIe slot version requirement	Maximum number of lanes with a 256-payload
Single	2 Gbytes/sec	PCle 2.x	4
Dual	4 Gbytes/sec	PCle 3.x	4
Quad CXP-6	4 Gbytes/sec	PCle 2.x	8
Quad CXP-12	8 Gbytes/sec	PCle 3.x	8
Pro Quad	8 Gbytes/sec	PCle 3.x	8

DMA write performance is chipset and computer dependent, and is slightly affected by the image size and alignment in Host memory.

The Matrox Rapixo CXP Host interface has four DMA write contexts, which act independently, simulating four DMA write engines running in parallel. The presence of multiple DMA contexts does not change the maximum bandwidth, but can help reduce latency.

Appendix A: Glossary

This appendix defines some of the specialized terms used in the Matrox Rapixo CXP documentation.

Glossary

Acquisition path.

A path that has the components to, for example, digitize or capture a video input signal. Some video sources require multiple acquisition paths.

ASPM.

Active State Power Management. A hardware PCIe mechanism that autonomously controls power consumption of the PCIe connectors in a computer. The actual power consumed by a PCIe device depends on the PCIe traffic and on the power-saving level to which the PCIe slot is configured. The power-saving level of the PCIe slot is initialized by the operating system.

Auxiliary I/O signals.

Auxiliary input/output signals. Non-video digital signals that can support one or more functionalities depending on the auxiliary signal (for example, trigger input or timer output). These signals are also known as general purpose I/O signals or GPIO signals.

Bandwidth.

A term describing the capacity to transfer data. Greater bandwidth is needed to sustain a higher transfer rate. Greater bandwidth can be achieved, for example, by using a wider bus or by increasing the clock frequency at which an interface or a processing core operates (for example, increasing the DDR4 SDRAM clock frequency).

HD-BNC connector.

High Definition Bayonet Neill-Concelman connector. A common connector used for 75 Ohm coaxial cables. Its fastener uses L-shaped slots to ensure that the coaxial cable is secured to the Matrox Rapixo CXP board.

CoaXPress.

An asymmetric high-speed communication standard used primarily for video and image data transfer. CoaXPress supports the transmission of video data, control signals, triggers, and power all on the same coaxial line. For each connection, CoaXPress supports downlink data rates of up to 12.5 Gbits/sec (1.25, 2.5, 3.125, 5.0, 6.25, and 12.5 Gbits/s) and an uplink data rate from 0.02 Gbits/s (21.33 Mbits/sec) to 0.4 Gbits/s (42.67 Mbits/sec).

• Contiguous memory.

A block of memory occupying a single, unbroken series of addresses.

CXP.

See CoaXPress.

DCF.

Digitizer configuration format. A file format that defines the input data format and, for example, how to accept or generate video timing signals, such as horizontal sync, vertical sync, and pixel clock.

DCF files have a .dcf extension.

DDR3 SDRAM.

Double-data-rate type 3 synchronous dynamic random-access memory. A type of general purpose consumer RAM. DDR3 SDRAM allows for data transfer at very high speeds, which is important for I/O-bound functions. This type of memory is inexpensive, high density, and very efficient as long as the data is accessed contiguously.

DDR4 SDRAM.

Double-data-rate type 4 synchronous dynamic random-access memory. A type of general purpose consumer RAM. DDR4 SDRAM allows for data transfer at very high speeds, which is important for I/O-bound functions. This type of memory is inexpensive, high density, and very efficient as long as the data is accessed contiguously.

• Digitizer configuration format.

See DCF.

Dynamic range.

The range of values present in a buffer. An unsigned 8-bit buffer, for example, has an allowable range of 0 to 255; its dynamic range can be any range within these values.

• Exposure time.

Refers to the period during which the image sensor of a video source is exposed to light. As the length of this period increases, so does the image brightness.

• Frame.

A single image grabbed from a video source.

Grab.

To acquire an image from a video source.

• Latency.

The time from when a command is sent to when its operation is started.

Linear encoder.

A device that provides information about the linear position and direction of a moving sensor along a scale, either as an analog or digital code.

LVDS.

Low-voltage differential signaling. LVDS offers a general-purpose, high bandwidth interface standard for serial and parallel data interfaces that require increased bandwidth at high speed, with low noise and power consumption.

• PCIe.

Peripheral Component Interconnect Express. The standard used for the computer bus that acts as an interface between hardware devices, such as Matrox Rapixo CXP, and your computer.

· Payload.

The amount of data transmitted to the PCIe bus within each data packet. Common payload sizes are 128, 256, 512, 1024, 2048, and 4096 bytes.

PoCXP.

Power-over-CoaXPress. Power-over-CoaXPress is the term for power transmitted to a video source over a coaxial cable using the CoaXPress standard. Power can be provided to a video source, at up to 13 W per cable, at a nominal voltage of 24 V.

• Quadrature decoder.

A device that decodes input received from a linear or rotary encoder with quadrature output.

• Real-time processing.

The processing of an image at the same speed or faster than the speed at which images are grabbed. Real-time processing ensures that no frames are missed.

Also known as live processing.

· Rotary encoder.

A device used to convert the angular position of a shaft or axle, to an analog or digital code.

• Timer output.

The signal generated by one of the programmable timers of the frame grabber. The timer output can be used to control external hardware. For example, it can be fed to the video source to control its exposure time or can be used to fire a strobe light.

Appendix B: Technical information

This appendix contains information that might be useful when installing your Matrox Rapixo CXP board.

Board summary

Global information

- Operating system: See your software manual for supported versions of Microsoft Windows and Linux.
- Minimum computer requirements:
 - A free PCIe slot. Note that for maximum bandwidth ensure that your PCIe slot has at least the following specifications:

Model	Number of PCIe lanes required*	PCIe slot version requirement (or later)*
Single	x4	PCIe 2.x
Dual	x4	PCle 3.x
Quad CXP-6	х8	PCle 2.x
Quad CXP-12	х8	PCIe 3.x
Pro Quad	х8	PCIe 3.x

- *. Note that you can install Matrox Rapixo CXP in any mechanical PCIe slot that fits your board (for example, connecting to open-ended connectors). Be aware that if you install it in a PCIe slot that has less PCIe lanes or is of an earlier version than the capabilities of the board, then the maximum bandwidth transfer rate will be affected. For example, you can install a x8 board in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Rapixo CXP and the Host is reduced by 50%.
- Processor with an Intel 64-bit architecture, or equivalent.
- A relatively up-to-date PCIe chipset. A chipset that supports the PCIe 2.x/3.x standard is preferable. The list of platforms that are known to be compatible with Matrox Rapixo CXP is available on the Matrox website, under the board's PC compatibility list.
- A proper power supply. Refer to the *Electrical specifications* section.

Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Technical features

- Supports 1, 2, or 4 independent CoaXPress connections, depending on the model. Image data can be transmitted at up to 6.25 Gbits/sec (Quad CXP-6) or up to 12.5 Gbits/sec (Single, Dual, Quad CXP-12, and Pro Quad) per connection.
- Supports frame-scan (area-scan) and line-scan video sources. The minimum and maximum number of pixels per line are 33 bytes and 16 Mbytes, respectively.
- Supports video sources with a Bayer color filter. Bayer color encoded images (GB, BG, GR, and RG pattern support) are converted to multi-band RGB images using a 2x2 average demosaicing algorithm.
- Can convert 8- or 16-bit monochrome data or 24- or 48-bit packed BGR data to 8- or 16-bit monochrome, 24- or 48-bit packed/planar BGR, 32-bit packed BGRa, 16-bit YUV (YUYV), or 16-bit YCbCr format.
- Provides power-over-CoaXPress (PoCXP), with up to 13 W per connection at a nominal voltage of 24 V, to any PoCXP-compliant device. For PoCXP on the Quad CXP-6, Quad CXP-12, and Pro Quad models, the internal auxiliary 12 V power connector must be connected to the computer's power supply cable that has a 6-pin, compatible, mating 12 V connector. The Single and Dual models use power from the PCIe slot to provide PoCXP; they do not need to be connected to an external power supply. The board is equipped with an overcurrent protection mechanism and a resettable fuse. The fuse can sustain a current of 1 A.
- Has 1 Gbytes (Single), 2 Gbytes (Dual), 4 Gbytes (Quad CXP-6/Quad CXP-12) or 8 Gbytes (Pro Quad) of DDR3 or DDR4 SDRAM. Total memory bandwidth of up to 6.4 Gbytes/sec (Single), 12.8 Gbytes/sec (Dual),14.9 Bytes/sec (Quad CXP-6),19.2 Gbytes/sec (Quad CXP-12), or 38.4 Gbytes/sec (Pro Quad).
- Has on-board programmable lookup tables (LUTs). These can map 8-bit, 10-bit, and 12-bit data (monochrome or color). When a link is receiving color data, all bands of the data use the same specified LUT mapping. As soon as one link is receiving 12-bit data, all links (CoaXPress connections) share the same specified LUT mapping. Data of greater depths are mapped through transparent LUTs.

- Can perform horizontal or vertical flipping.
- Can subsample image data using nearest neighbor integer subsampling factors of 1 to 16.
- Has a Processing FPGA (only Pro Quad) for on-board, custom processing.
 Processing units (PUs) can be Matrox developed, or user developed using the
 Vivado HSL tool of the Xilinx Vivado Design Suite and Matrox FPGA
 Development Kit (FDK).
- Has 32 (Quad CXP-6, Quad CXP-12, and Pro Quad) or 24 (Single and Dual) auxiliary signals (with the cable adapter bracket installed) that are path independent. Each auxiliary I/O connector (HD-15) provides the following number of signals:
 - 3 TTL auxiliary I/O signals (trigger input or user input signals, or timer output, re-routing of the CoaXPress trigger input, or user output signals).
 - 1 LVDS auxiliary output signal (timer output, re-routing of the CoaXPress trigger input, or user output signals).
 - 2 LVDS auxiliary input signals (trigger input, rotary/linear encoder input, or user input signals).
 - 2 opto-isolated auxiliary input signals (trigger input signals).

Auxiliary input signals (or auxiliary I/O signals set to input) can be rerouted to the CoaXPress trigger output signal and the auxiliary output signals.

The auxiliary input signals have interrupt generation capabilities. In addition, when the LVDS auxiliary input signals are used for rotary/linear encoder input, they can be debounced.

- Has 4 quadrature decoders. Each supports external 5 V linear or rotary encoders with quadrature output*, and frequencies of up to 50MHz.
- Has 4 general timers. Each timer is a 16-bit timer that can count up to 65,535 clock ticks before resetting. Each timer uses 125 MHz internal clock source.
- Supports coaxial cable lengths of up to 60m running at 6.25 Gbits/sec and 40m running at 12.5 Gbits/sec, depending on the number of cameras connected. See *Appendix 4: Performance* for more information.
- Has a CoaXPress LED for each CoaXPress input connector, to identify the status and activity of each connected device.
- Has 4 board status LEDs: board-power good, board configuration, PCIe speed/#lanes, and fallback board configuration.
- A fanless design on all base models (Quad CXP-6, Single, Dual, and Quad CXP-12).
- Support for MIL license fingerprint and storage.

^{*.} Maximum differential swing of 3 V.

Electrical specifications

The following table describes electrical specifications for the Matrox Rapixo CXP.

Operating voltage and current for Matrox Rapixo CXP							
Quad CXP-6 and Quad CXP-12	Typical: 3.3 V, 0.1 A mA (330 mW)						
	Typical 12.0 V, 1.4 A (17 W)						
	Max. PoCXP 18.5 - 24.0 V, 700 mA: 13 W (Current drawn from the internal auxiliary 12 V power connector. Power is not dissipated by the board; it is only used by the video source).						
	Total dissipated by the board: $0.33 \text{ W} + 17 \text{ W} = 17.33 \text{ W}$ (typical)						
	Total dissipated by board and PoCXP video sources = 17.33 W + (4 * 17 W) = 85.33 W (typical)						

The following table describes the specifications for the auxiliary I/O signals on Matrox Rapixo CXP.

I/O Specifications						
Input signals in LVDS	100 Ohm differential termination.					
format	nput voltage on the (+) or (-) pin: -4 V (min) to +5 V (max).					
	Maximum differential input: 3 V.					
Output signals in LVDS	Expecting a load of 100 Ohms.					
format	Differential output voltage (with load of 100 Ohm): 250 mV (min) to 450 mV (max).					
	Offset voltage (common-mode): 1.125 V (min) to 1.375 V (max).					
Input signals in TTL format	No series termination.					
	Pulled up to 3.3 V with 4.7 KOhm.					
	Clamped to -0.7 V to +5.7 V.					
	Input voltage: low of 0.8 V (max); high of 2.0 V (min).					
Output signals in TTL	27 Ohm series termination.					
format	High-level output current: -32 mA (max).					
	Low-level output current: +64 mA (max).					
	High-level output voltage: 2.0 V (min).					
	Low-level output voltage: 0.55 V (max).					
Opto-coupled input signals	511 Ohm series termination (connected on the anode inputs of the opto-coupler device).					
	High-level Input current threshold: 5 mA (min) to 15 mA (max) (6.3 mA to 10 mA recommended).					
	Input voltage: low (V _{il}) of 0.8 V (max); high (V _{ih}) of 4.71 V (min) to 9.165 V (max).					
	Input forward voltage (at 25 degrees C): 1.3 V (min), 1.8 V (max).					
	Propagation delay (at 25 degrees C): 100 ns (max).					

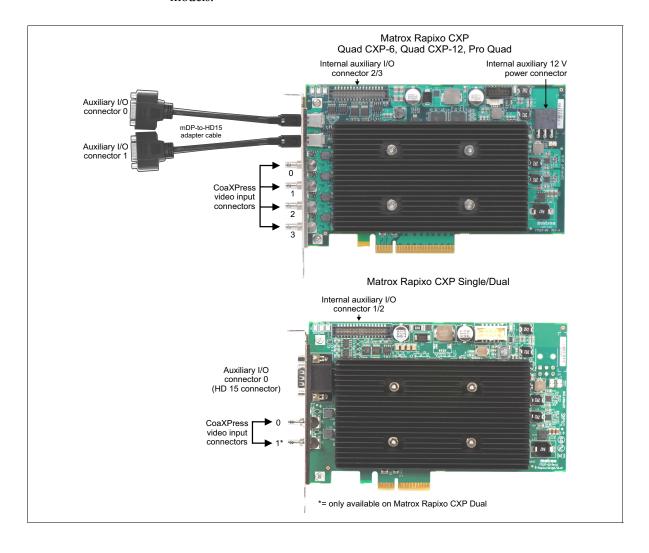
Dimensions and environmental specifications

- Dimensions of all Matrox Rapixo CXP boards: 16.76 L x 11.12 H x 1.871 W cm (6.6" x 4.376" x 0.737") from bottom edge of goldfinger to top edge of board. These values respect the dimensions of a PCIe half-length board.
- Ventilation: 150 LFM over board(s) (through the heat sink) in a single board configuration. More ventilation might be required in multiple board configurations.
- Minimum/maximum ambient operating temperature *: 0°C to 55°C (32°F to 131°F).
- Minimum/maximum storage temperature: -40°C to 75°C (-40°F to 167°F).
- Operating relative humidity: up to 95% relative humidity (non-condensing).
- Storage humidity: up to 95% relative humidity (non-condensing).

^{*.} In the vicinity of the board.

Connectors on the Matrox Rapixo CXP board

On the Matrox Rapixo CXP board, there are several connectors. On the bracket of the main board, there are up to four CoaXPress video input connectors and up to two mDP connectors. In addition, close to the top edge of the main board, there is an internal auxiliary I/O connector. An internal auxiliary 12 V power connector is also available on the Quad CXP-6, Quad CXP-12, and Pro Quad models.



The mDP-to-HD15 adapter cable connects to a mDP connector on the main bracket. If the cable is attached to the top mDP connector, the HD-15 connector at the end of this cable is called external auxiliary I/O connector 0; otherwise, it is called external auxiliary I/O connector 1. Note that only one mDP-to-HD15 adapter cable is included with the board; you can optionally purchase a second adapter cable.

The optional cable adapter bracket provides 2 additional external auxiliary I/O connectors (HD-15). Auxiliary I/O connectors 1 and 2 are found on the cable adapter bracket of the Single and Dual models, and auxiliary I/O connectors 2 and 3 are found on the cable adapter bracket of the Quad CXP-6, Quad CXP-12, and Pro Quad. The cable adapter bracket attaches to this internal auxiliary I/O connector.

CoaXPress video input connectors

The CoaXPress (CXP) video input connectors are 75 Ohm, 12G rated, high-density BNC (HD-BNC/micro-BNC) female connectors (jack). They are used to receive video input streams and send and receive CoaXPress trigger signals, as well as control and acknowledgment messages.

To interface with these connectors, use 75 Ohm coaxial cables with a 12G rated, HD-BNC male connector (plug). You can purchase high-quality, 75 Ohm coaxial cables from your video source manufacturer, Belden Inc., or other third parties. Note that these cables are not available from Matrox.

When using more than one CoaXPress cable to connect to the same video source, you must choose cables of the same type and length, to ensure that the cables have the same propagation delay.

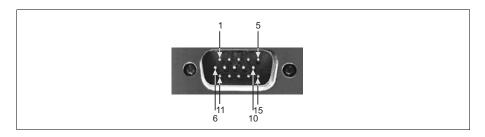
Video sources can be connected to the CoaXPress video input connectors in any order. Matrox Rapixo CXP communicates with the video source(s) to identify which video source is connected to which connector(s).

External auxiliary I/O connectors

The external auxiliary I/O connectors on the mDP-to-HD15 adapter cable and the cable adapter bracket are high-density D-subminiature 15-pin (HD-15*) male connectors. The external auxiliary I/O connectors are used to transmit and receive auxiliary signals.

- ❖ The auxiliary I/O connectors on Matrox Rapixo CXP are not compatible with display devices. Connecting one of the HD-15 connectors to a VGA monitor or any other display device might damage both the device and the Matrox Rapixo CXP board.
- In addition, the mDP connectors directly on the Matrox Rapixo CXP bracket are not compatible with a DisplayPort source. Connecting one of the mDP connectors to such a device might damage both the device and the Matrox Rapixo CXP board.

The auxiliary signals are path independent; regardless of the acquisition path that is being used to grab images, any of the auxiliary signals can be used. For more information, see the Auxiliary signals section in Chapter 4: Matrox Rapixo CXP hardware reference chapter for supported functionality.



^{*.} Previously referred to as DBHD-15, but more accurately known as DE-15.

The pinout for auxiliary I/O connector 0 is as follows. Auxiliary I/O connectors 1, 2, and 3* have the same pinout as auxiliary I/O connector 0, except you must add 8, 16, or 24, respectively, to the number at the end of their hardware signal name and MIL constant. For example, AUX(TRIG)_TTL_IO_4 on connector 0 would be AUX(TRIG)_TTL_IO_12 on connector 1.

Pin	Hardware signal name	MIL constant for auxiliary signal	Description	
1	AUX(TRIG)_TTL_I0_4	M_AUX_IO4	TTL auxiliary signal 4 (input/output), which supports: timer output (M_TIMER1/M_TIMER2/M_TIMER3/M_TIMER4), trigger input, user input, or use output (M_USER_BIT4).	
2	AUX(TRIG)_TTL_I0_5	M_AUX_I05	TTL auxiliary signal 5 (input/output), which supports: timer output (M_TIMER1/M_TIMER2/M_TIMER3/M_TIMER4), trigger input, user input, or user output (M_USER_BIT5).	
3	AUX(TRIG)_TTL_I0_6	M_AUX_I06	TTL auxiliary signal 6 (input/output), which supports: timer output (M_TIMER1/M_TIMER2/M_TIMER3/M_TIMER4), trigger input, user input, or use output (M_USER_BIT6).	
4+,5-	AUX(TRIG)_LVDS_IN2	M_AUX_I02	LVDS auxiliary signal 2 (input), which supports: trigger input, user input, or rotary/linear encoder input bit 0.	
6+,8-	AUX(TRIG)_LVDS_IN3	M_AUX_I03	LVDS auxiliary signal 3 (input), which supports: trigger input, user input, or rotary/linear encoder input bit 1.	
7	GND	N/A	Ground.	
10	GND	N/A	Ground.	
12+,11-	AUX(TRIG)_OPTO_IN1	M_AUX_I01	Opto-isolated auxiliary signal 1 (input), which supports: trigger input or user input.	
13+,14-	AUX(EXP)_LVDS_OUT7	M_AUX_I07	LVDS auxiliary signal 7 (output), which supports: timer output (M_TIMER1/M_TIMER2/M_TIMER3/M_TIMER4) or user output (M_USER_BIT7).	
15+,9-	AUX(TRIG)_OPTO_IN0	M_AUX_I00	Opto-isolated auxiliary signal 0 (input), which supports: trigger input or user input.	

To build your own cable, you can purchase the following parts:

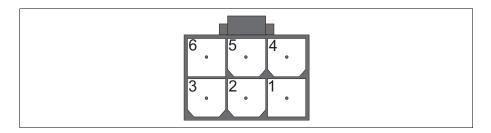
	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

^{*.} Only available on the Quad CXP-6, Quad CXP-12, and Pro Quad models.

Internal auxiliary 12 V power connector

The internal auxiliary 12 V power connector available on the Quad CXP-6, Quad CXP-12, and Pro Quad models. The internal auxiliary 12 V power connector Matrox Rapixo CXP is a standard 6-pin, 12 V connector. If this connector is attached to the computer's power supply cable that has a 6-pin, compatible, mating 12 V connector, Matrox Rapixo CXP can provide power-over-CoaXPress (PoCXP) to the devices connected to the CoaXPress input connectors, at up to 13 W per connection at a nominal voltage of 24 V.



The pinout for the auxiliary 12 V power connector is as follows:

Pin	Description
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

Status LEDs on Matrox Rapixo CXP

Matrox Rapixo CXP has LEDs to display the status of the CoaXPress connections and the board.

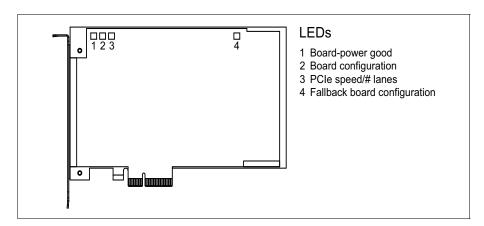
CoaXPress LEDs

Matrox Rapixo CXP has one CoaXPress LED per video input (HD-BNC) connector. Each LED indicates the connection status between the device (camera) plugged into the LED's associated connector and the Host (frame grabber). Each LED also indicates whether the device is sending data, and whether Matrox Rapixo CXP is transmitting power to the device.

LED color and state	Description		
Off	Matrox Rapixo CXP is not receiving power.		
Orange, solid	Matrox Rapixo CXP is booting. The PoCXP-device sensing circuitry has not been enabled yet.		
Red, slow pulse	Matrox Rapixo CXP driver has started, but nothing is connected.		
Alternating green/orange, fast flash	Matrox Rapixo CXP has detected a PoCXP-compliant connection.		
Orange, fast flash	Matrox Rapixo CXP has detected a non-PoCXP compliant connection. PoCXP is disabled.		
Alternating red/green, slow flash	The device is incompatible; PoCXP is enabled.		
Alternating red/orange, slow flash	The device is incompatible. PoCXP is disabled.		
Red, solid	Overcurrent was detected in the PoCXP circuitry, possibly because of a failure in the connected device or damage to the cable. Matrox Rapixo CXP stopped sending power to the device to avoid damaging the device or the board.		
Green, solid	The device is compatible and Matrox Rapixo CXP has established a connection with the device (on the specified cable). Note that this requires an MdigAlloc() call. No data is being transferred.		
Orange, slow pulse	Matrox Rapixo CXP is waiting for a grab trigger. Note that this state only occurs in triggered grab mode.		
Green, fast flash	Matrox Rapixo CXP is receiving data from the connected device.		
Red, 500 ms pulse	An error occurred during data transfer.		
Red, fast flash	A CoaXPress system error occurred on the Matrox Rapixo CXP board. This type of error can prevent Matrox Rapixo CXP from receiving data. For example, an error will occur if the internal auxiliary 12 V power connector is not connected to a power source.		

Board status LEDs

Matrox Rapixo CXP has four board status LEDs to indicate the status of the board: board-power good, board configuration, PCIe speed/#lanes, and fallback board configuration.



The table below outlines the possible colors for each LED and their definitions.

LED	LED color and state	Description		
1. Board-power good	Off/Red	One or more of the on-board voltage regulators did not start.		
		If your computer is on and this LED state occurs, there is an issue with the voltage regulators on your Matrox Rapixo CXP. Contact Matrox technical support.		
	Green	All of the on-board voltage regulators are working properly.		
2. Board configuration	Red	The board is not configured.		
	Green	The board is configured.		
3. PCle speed/# lanes	Off	The PCIe link is down.		
	Blinking red	Slot is PCle 1.x and not all lanes are active.		
	Blinking orange	Slot is PCle 2.x and not all lanes are active.		
	Blinking green	Slot is PCle 3.x and not all lanes are active.		
	Solid red	Slot is PCle 1.x and all lanes are active.		
	Solid orange	Slot is PCle 2.x and all lanes are active.		
	Solid green	Slot is PCIe 3.x and all lanes are active.		
4. fallback board	Off	The normal board configuration is being used.		
configuration	On	The normal board configuration was corrupt. The fallback (golden) board configuration is being used.		

Appendix C: Listing of Matrox Rapixo CXP boards

This appendix lists the key feature changes to the Matrox Rapixo CXP boards.

Key feature changes

Part number	Version	Description	
RAP1G1C12	000	First shipping version of Matrox Rapixo CXP Single PCIe 2.1 x4 frame grabber with 1 Gbyte DDR3 SDRAM.	
RAP2G2C12 000 First shipping version of Matrox Rapixo CXP Dual Figrabber with 2 Gbytes DDR3 SDRAM.		First shipping version of Matrox Rapixo CXP Dual PCle 3.1 x4 frame grabber with 2 Gbytes DDR3 SDRAM.	
RAP4G4C6	000	First shipping version of Matrox Rapixo CXP Quad CXP-6 PCIe 2.1 x8 frame grabber with 4 Gbytes DDR4 SDRAM.	
	100	Added jumper that forces fallback to golden firmware.	
RAP4G4C12	000	First shipping version of Matrox Rapixo CXP Quad CXP-6 PCle 3.1 x8 frame grabber with 4 Gbytes DDR4 SDRAM.	
	100	Added jumper that forces fallback to golden firmware.	
RAP8G4C12P352	000	First shipping version of Matrox Rapixo CXP Pro Quad CXP-12 PCIe 3.1 x8 frame grabber with 8 Gbytes DDR4 SDRAM and Xilinx Kintex Ultrascale KU035 FPGA.	
	100	Added jumper that forces fallback to golden firmware.	
RAP8G4C12P602	000	First shipping version of Matrox Rapixo CXP Pro Quad CXP-12 PCIe 3.1 x8 frame grabber with 8 Gbytes DDR4 SDRAM and Xilinx Kintex Ultrascale KU060 FPGA.	
	100	Added jumper that forces fallback to golden firmware.	

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Regulatory Compliance

FCC Compliance Statement

Warning

Changes or modifications to these devices not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

The use of shielded cables for connections of these devices to other peripherals is required to meet the regulatory requirements.

Note

These devices comply with Part 15 of FCC Rules. Operation is subject to the following two conditions:

- 1. These devices may not cause harmful interference, and
- 2. These devices must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for Class A digital devices, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of these devices in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

Innovation, Science and Economic Development Canada Compliance Statement

These digital apparatuses do not exceed the Class A limits for radio noise emission from digital apparatuses set out in the Radio Interference Regulations of Innovation, Science and Economic Development Canada (ISED).

Ces appareils numériques n'émettent pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par Innovation, Sciences et Développement Économique Canada (ISDE).

EU Notice (European Union)

WARNING: These are class A products. In a domestic environment these products may cause radio interference in which case the user may be required to take adequate measures.

AVERTISSEMENT: Ces appareils sont des produits informatiques de Classe A. Lorsque ces appareils sont utilisés dans un environnement résidentiel, ces produits peuvent entraîner des interférences radioélectriques. Dans ce cas, l'usager peut être prié de prendre des mesures correctives appropriées.

This device complies with Directive 2014/30/EU for Class A digital devices. They have been tested and found to comply with EN55032/CISPR32 and EN55024/CISPR24 when installed in a typical class A compliant host system. It is assumed that these devices will also achieve compliance in any Class A compliant system.

Ces unités sont conformes à la Directive 2014/30/EU pour les unités numériques de Classe A. Les tests effectués ont prouvé qu'elles sont conformes aux normes EN55032/CISPR32 et EN55024/CISPR24 lorsqu'elles sont installées dans un système hôte typique de la Classe A. On suppose qu'ils présenteront la même compatibilité dans tout système compatible de la Classe A.

Directive on Waste Electrical and Electronic Equipment (WEEE)

Europe

(English) European user's information – Directive on Waste Electrical and Electronic Equipment (WEEE)

Please refer to the Matrox Web site (www.matrox.com/environment/weee) for recycling information.



(Français) Informations aux utilisateurs Européens – Règlementation des déchets d'équipements électriques et électroniques (DEEE)

Se référer au site Web de Matrox (www.matrox.com/environment/weee) pour l'information concernant le recyclage.

(Deutsch) Information für europäische Anwender – Europäische Regelungen zu Elektro- und Elektronikaltgeräten (WEEE)

Bitte wenden Sie sich an dem Matrox-Website (www.matrox.com/environment/weee) für Recycling Informationen.

(Italiano) Informazioni per gli utenti europei – Direttiva sui rifiuti di apparecchiature elettriche ed elettroniche (RAEE)

Si prega di riferirsi al sito Web Matrox (www.matrox.com/environment/weee) per le informazioni di riciclaggio.

Limited warranty

Refer to the warranty statement that came with your product.